REMARKS

Claims 1-22 were originally filed in the present application.

Claims 1-22 are pending in the present application.

Claims 1-22 were rejected in the September 17, 2007 Office Action.

No claims have been allowed.

Reconsideration of the claims is respectfully requested.

Applicant thanks the Examiner for the new final Office Action, as the incorrectly checked box did lead Applicant to believe that no further action was necessary and a Notice of Allowance would be forthcoming. The Examiner's further comments have been considered and are addressed below.

In the September 17, 2007 Office Action, the Examiner rejected Claims 1-22 under 35 U.S.C. §102(b) as being anticipated by U. S. Patent No. 6,192,051 to *Lipman al.* (hereafter, simply "*Lipman*").

Independent claims 1 and 11 each require "a first portion of said first received address accesses an address table in a first memory circuit and an output of said first memory circuit accesses an address table in a second memory circuit". This feature is not taught or suggested by Lipman.

While Lipman's Figure 11 does show that IP address bits [31:16] provide the index of an entry in the level-1 tree 150 (col. 15, lines 59-61), the output "Next Tree Index" (the "NT pointer") is not used to "access[] an address table in a second memory circuit" where the second memory circuit is one of the "M pipelined memory circuits", as claimed in Claims 1 and 11. Instead, the NT pointer

from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

Figure 11 shows that the NT pointer from the level-1 tree 150 is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67), and nothing teaches or suggests that the forwarding table . That is, rather than being used to access the next memory circuit in a pipeline of memory circuits forming a trie table, it appears to be used for a separate lookup as an index in a forwarding table. The output of that forwarding table appears to be used as an offset index, added to T2 base, into the level-2 tree 154.

The Examiner now indicates that he believes that element 144 portion "128.63" satisfies the claimed "first portion of said first received address". On the contrary, Lipman describes that "A portion of the level 1 tree 140 is shown in FIG. 7, including locations 128.63 through 128.68." *Col. 10, lines 59-60.* Applicant assumes that this is a typographic error in the patent, and the reference to "140" should be to "144".

The Examiner also indicates that Lipman's next tree table 152 is the claimed "address table in the second memory circuit". Of course, by combining element 144 from Figure 7 and element 152 of Figure 11, the Examiner is unable to show at all that there are any pipelined memory circuits, as

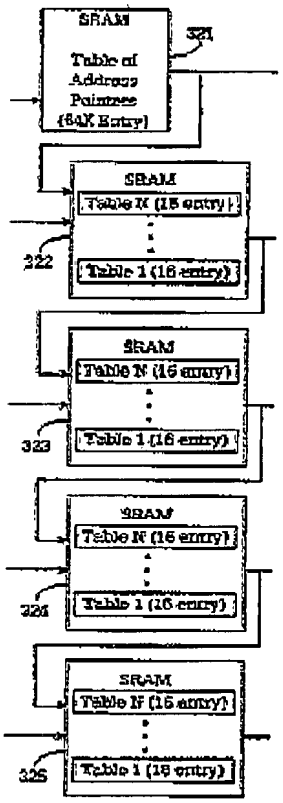
these two figures do not show any common elements interrelating. Figure 11 is describing a compressed tree, Figure 7 is describing an uncompressed tree, and these do not interrelate.

The Examiner now responds with a broad interpretation of "memory circuit" that describes "a combination of interconnected electrical components or pathways that perform a specific task, that being data storage", and indicates that these are shown in Figure 8. Figure 8 shows a data structure, by Lipman's own description, not any interconnected electrical components or pathways corresponding to the Examiner's own definition. Figure 7 is also a data structure. Data structures are not memory circuits.

Certainly a data structure is stored in a physical memory comprising memory circuits. However, a typical physical memory is not comprised of pipelined memory circuits, and certainly not in the manner claimed. Nothing in Lipman describes pipelined memory circuits as claimed.

In fact, though Lipman shows multiple tables that point to each other, nothing in Lipman's description teaches or suggests a lookup circuit comprising "M pipelined memory circuits" as claimed. The Examiner's statement that "these memory circuits are 'pipelined' in that they each point to another circuit" is not persuasive. Those of skill in the art recognize that a "pipeline" is a series of elements each connected so that the output of one element is an input of the next element. See, for example, Figure 3 of the present application, reproduced below, where the output of each pipelined SRAM is an input to the next one in series. Lipman does not appear to teach or suggest such a pipeline at all, much less pipelined memory circuits.

A portion of Figure 3 of the instant application is reproduced below. Note that SRAM 321 is pipelined with 322, 323, 324, and 325, in that each memory circuit has an output connected to the input of the next memory circuit.



The Examiner refers to Lipman's Figure 7 for "pipelined memory circuits", but this figure shows a diagram of a data structure, not memory circuits. If the Examiner is intending to imply that the actual semiconductor circuits that comprise each bit/cell of a memory are the "memory circuits",

then the Examiner will surely recognize that these are not typically pipelined, and Lipman certainly doesn't teach any such pipelining. Lipman doesn't teach series connections or pipelining of memory circuits at all.

The Examiner responds that "Lipman teaches pipelining via the levels of the 'tree' that are accessed in sequence. For example, a first tree level is accessed, followed by a second level, and third (i.e. a pipeline)." The Examiner's response illustrates his misunderstanding. The sort of sequential access described by the Examiner is not a pipeline, as recognized by those of skill in the art. In a pipeline, data passes from a first element, directly to the next element, and then directly to the element after that. This is very different from, for example, a processor that sends data to/from a first element, then sends data to/from a second element, then sends data to/from a third element. A pipeline of elements is connected in series, not merely accessed in sequence.

The Examiner's statement that "Pipelining is a term which is used to identify strings of several data or objects" is simply incorrect, particularly as applied to "strings of data". The Examiner is requested to cite the source of this remarkable definition.

As such, Lipman does not anticipate independent claims 1 or 11, or their respective dependent claims 2-10 and 12-20.

Claim 21 requires that the output from the address table in the first memory circuit is a first address pointer that indexes a start of an address table in a second memory circuit. Claims 2 and 12 include similar limitations. These features are not taught or suggested by Lipman.

As described above, the output of the level-1 tree 150 (the NT pointer) is used as an index into the level-2 next tree table 152 of the forwarding table (col. 15, lines 65-67). Lipman also describes that the base of the level-2 next tree table 152 is pointed to by the level 2 pointer 218 from the level pointer block 210. As such, it is clear that the NT pointer does not index a start of the address table in the second memory circuit, as claimed. As such, it is clear that Lipman also does not teach or suggest the features of claims 2, 12, or independent claim 21. Claim 21 also requires M pipelined memory circuits, not taught or suggested by Lipman. Lipman similarly does not teach or suggest the features of dependent claim 22. These rejections are traversed.

The undersigned would welcome an opportunity to resolve any remaining issues via telephone, to expedite allowance of this case.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of the pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: November 16, 2007

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